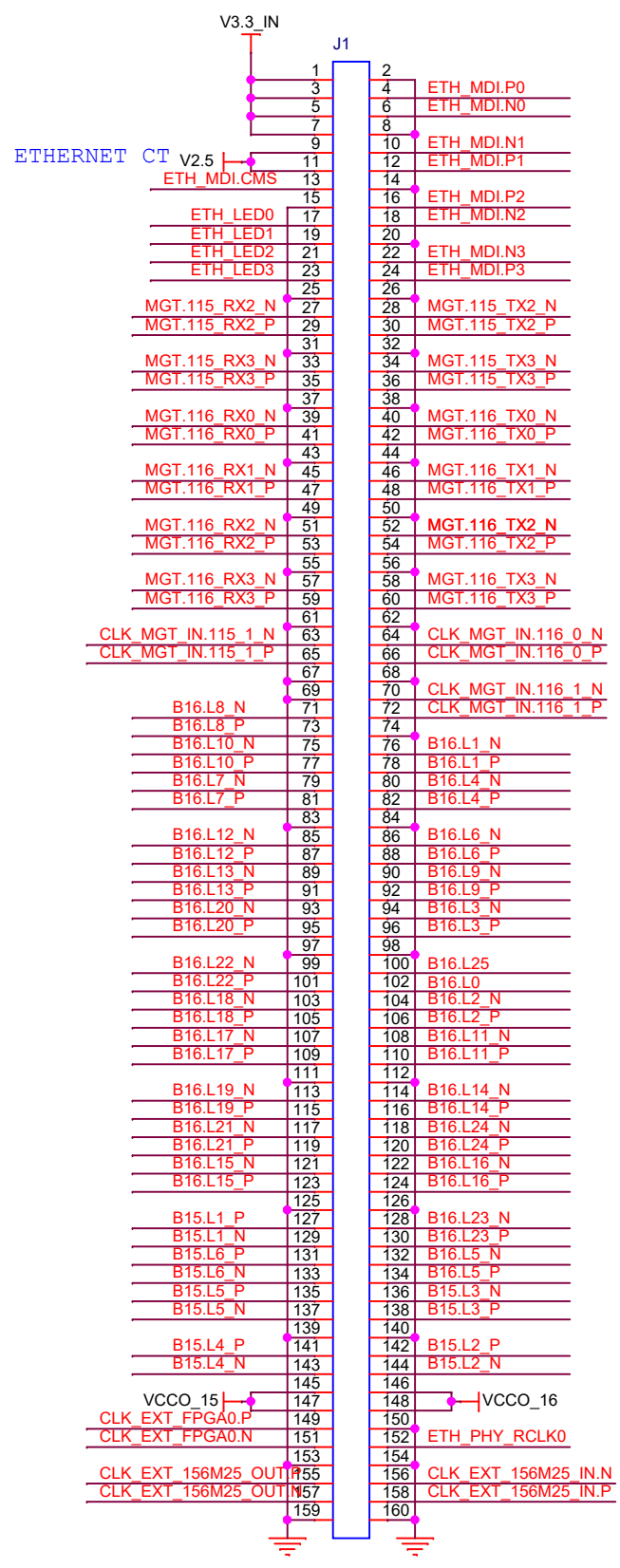


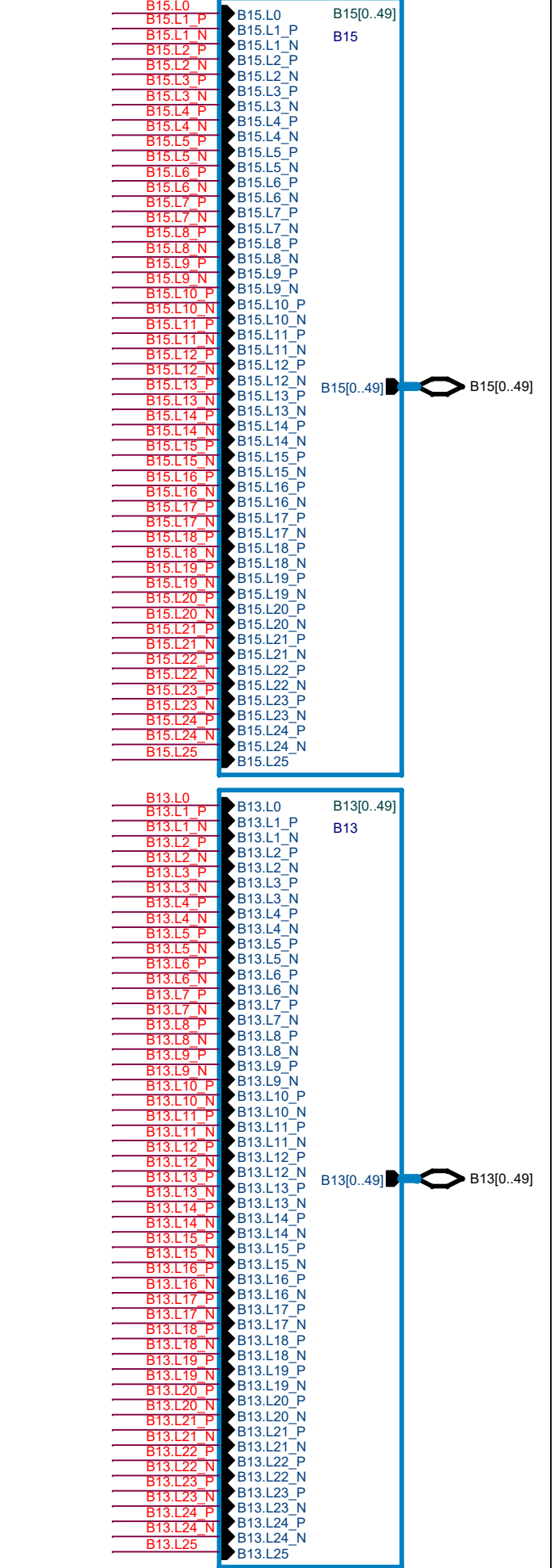
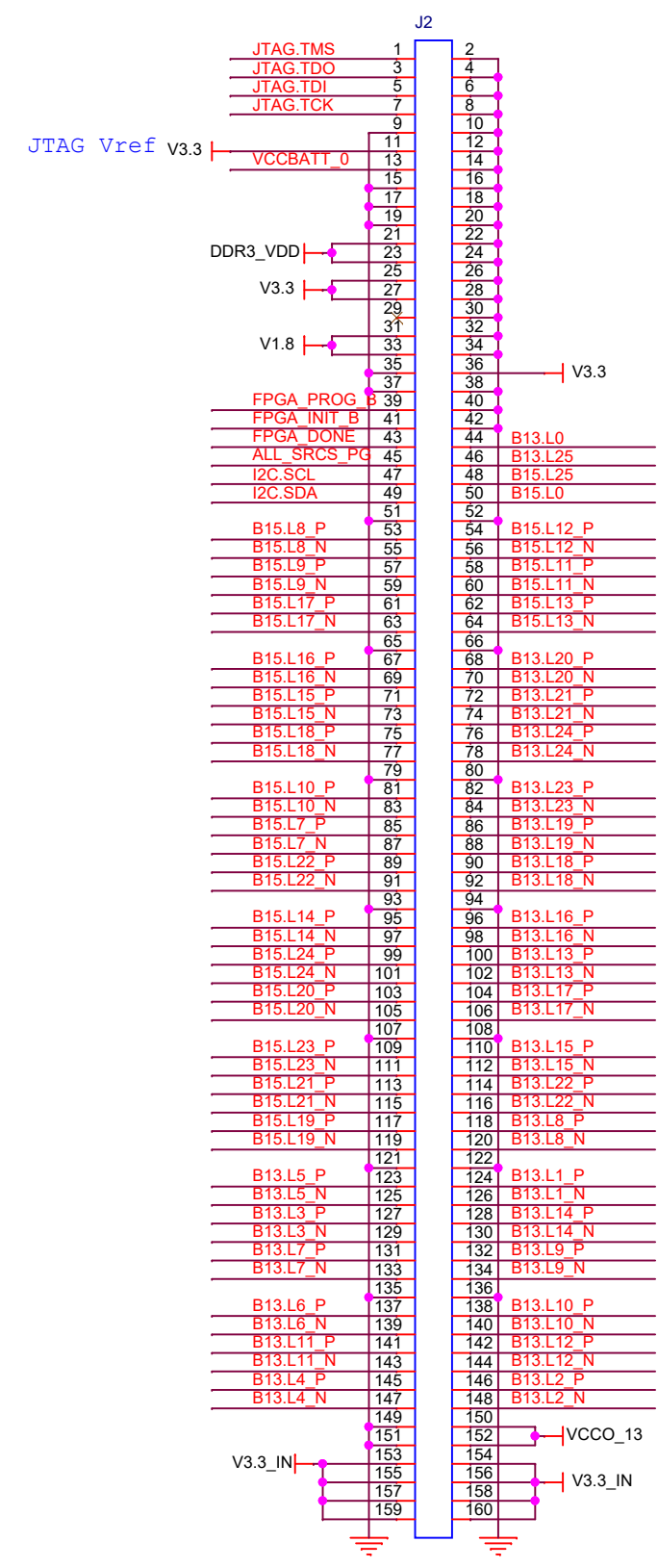
3.3V signals (LVCMOS33)

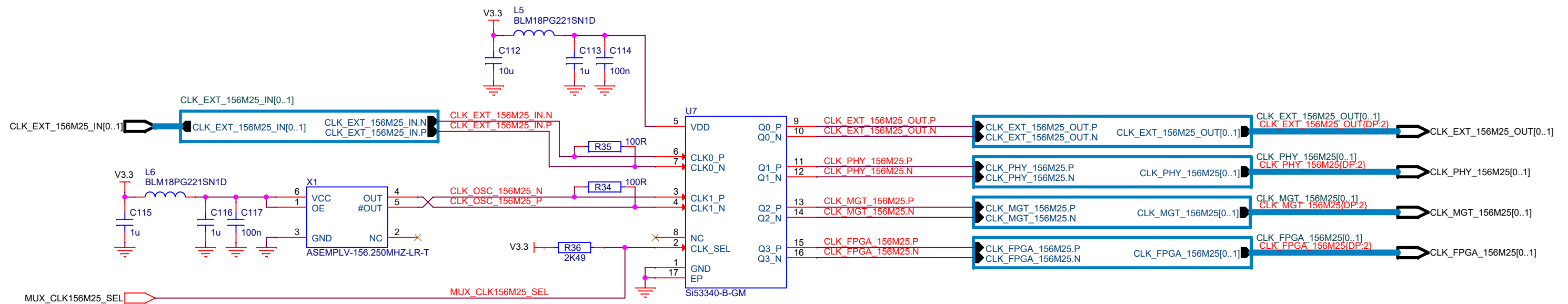
LVDS



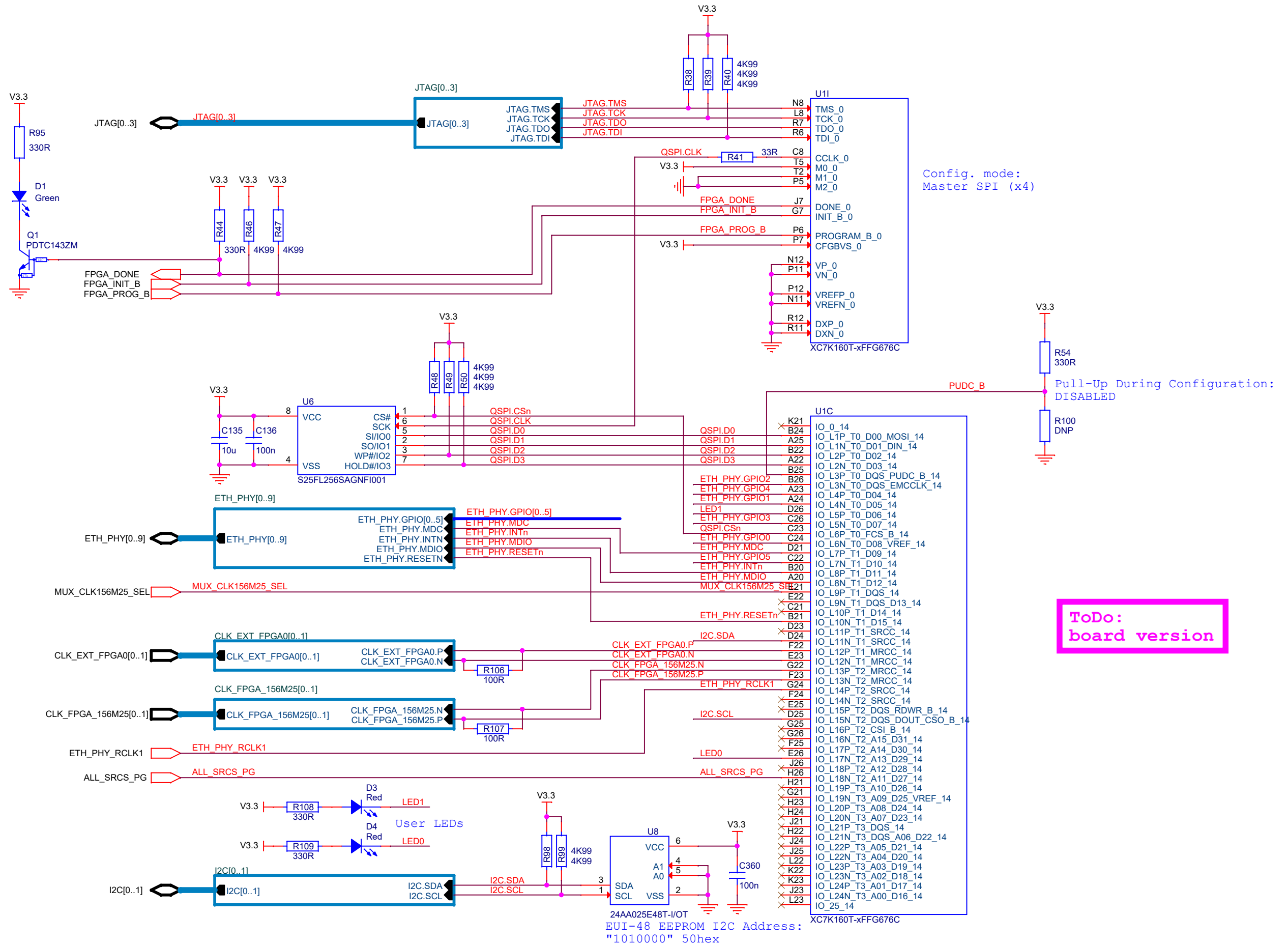
Module power supplies inputs/outputs description:

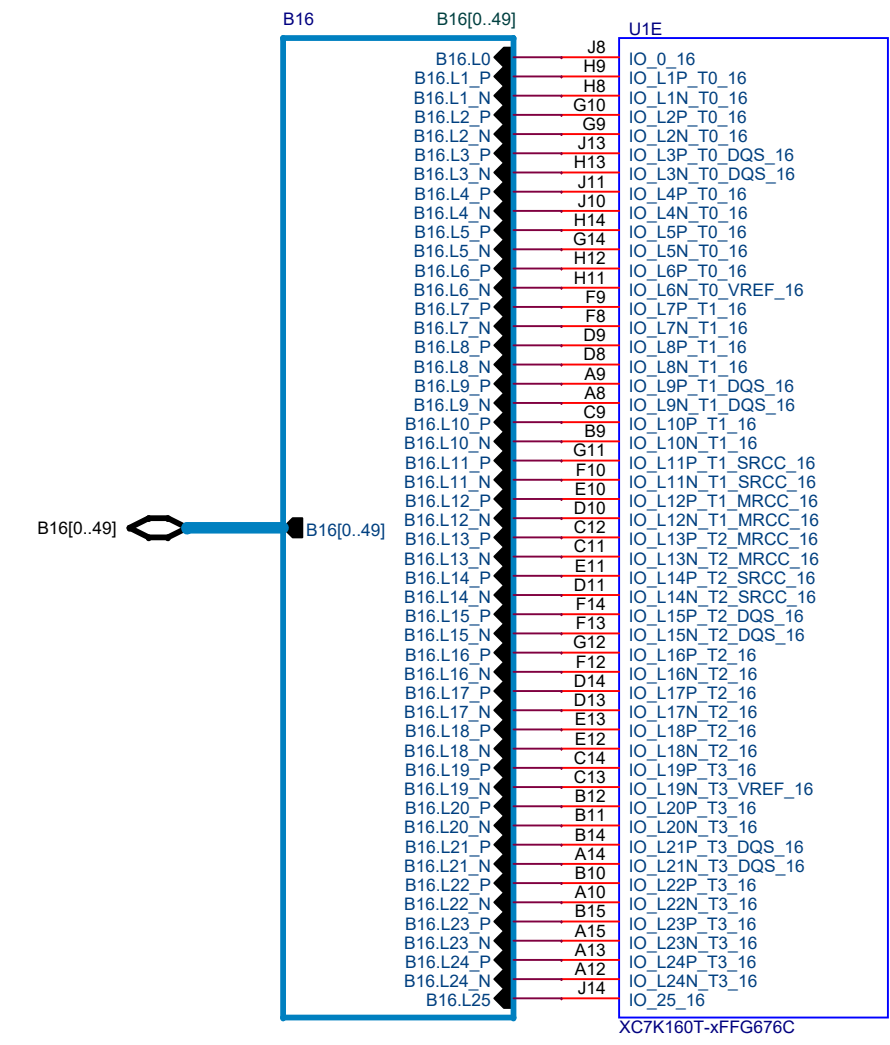
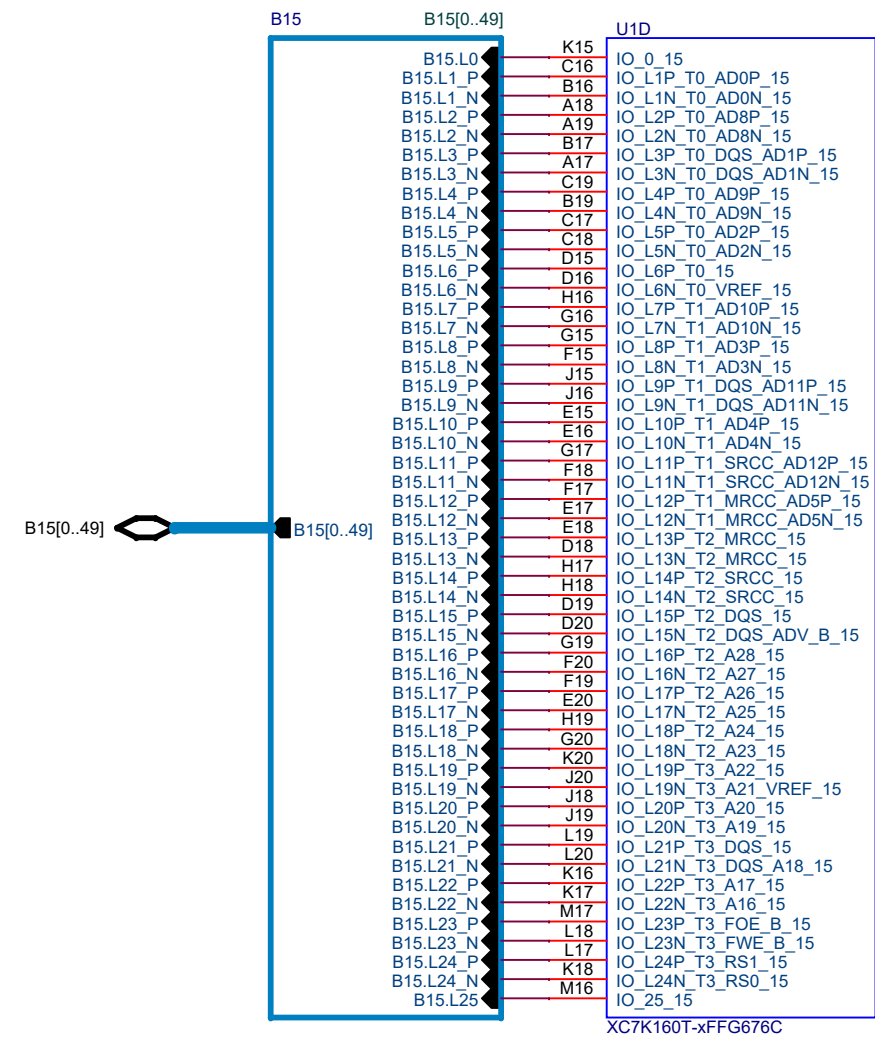
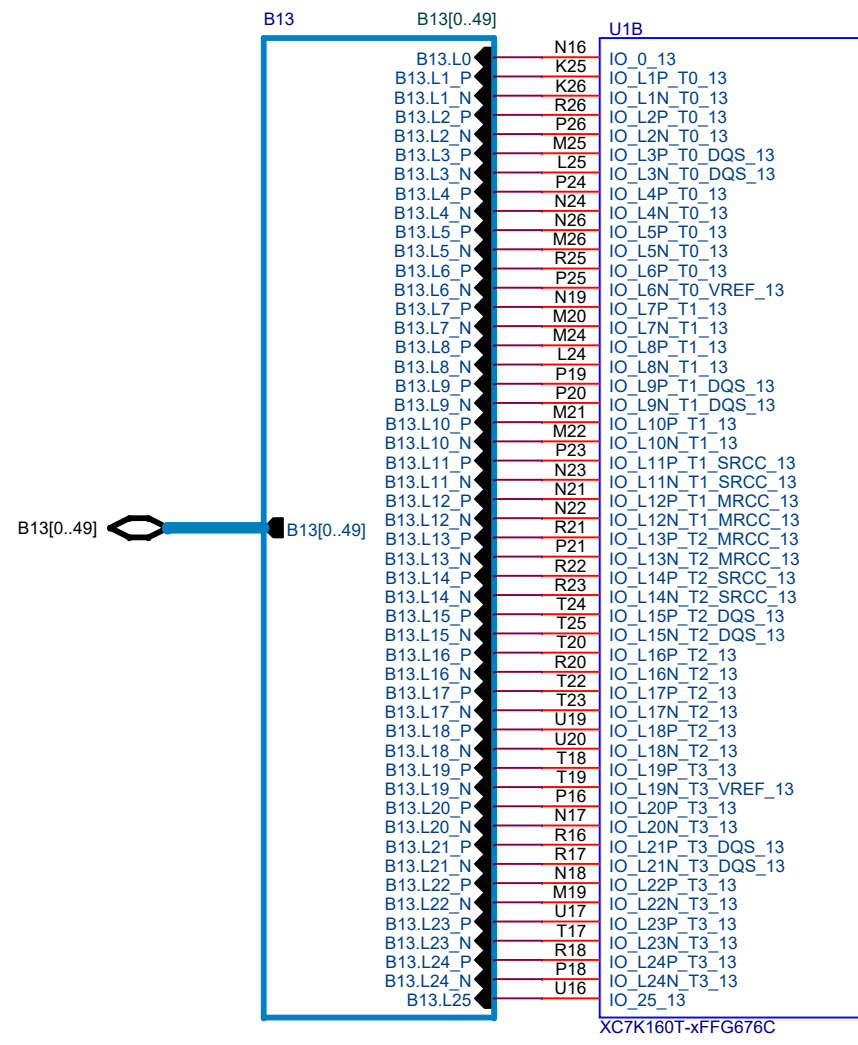
V3.3_IN	V3.3_IN	Board PWR input 3.3V (+5/-0 %)
VCCO_13	VCCO_13	
VCCO_15	VCCO_15	FPGA IOBank 13, 15 and 16 VCCO inputs (1.2V to 3.3V)
VCCO_16	VCCO_16	
VCCBATT_0	VCCBATT_0	Connect to GND or 1.8V (backup battery or V1.8)
V3.3	V3.3	3.3V output & JTAG Vref (max. 0.5A)
V2.5	V2.5	2.5V output & Ethernet CT(max. 0.5A)
V1.8	V1.8	1.8V output (max. 0.5A)
DDR3_VDD	DDR_VDD	1.35/1.5V output (max. 0.5A)



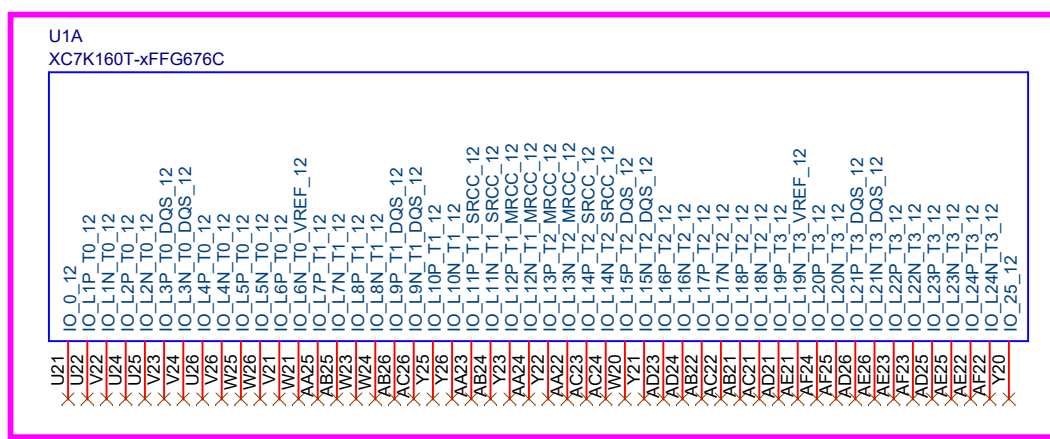


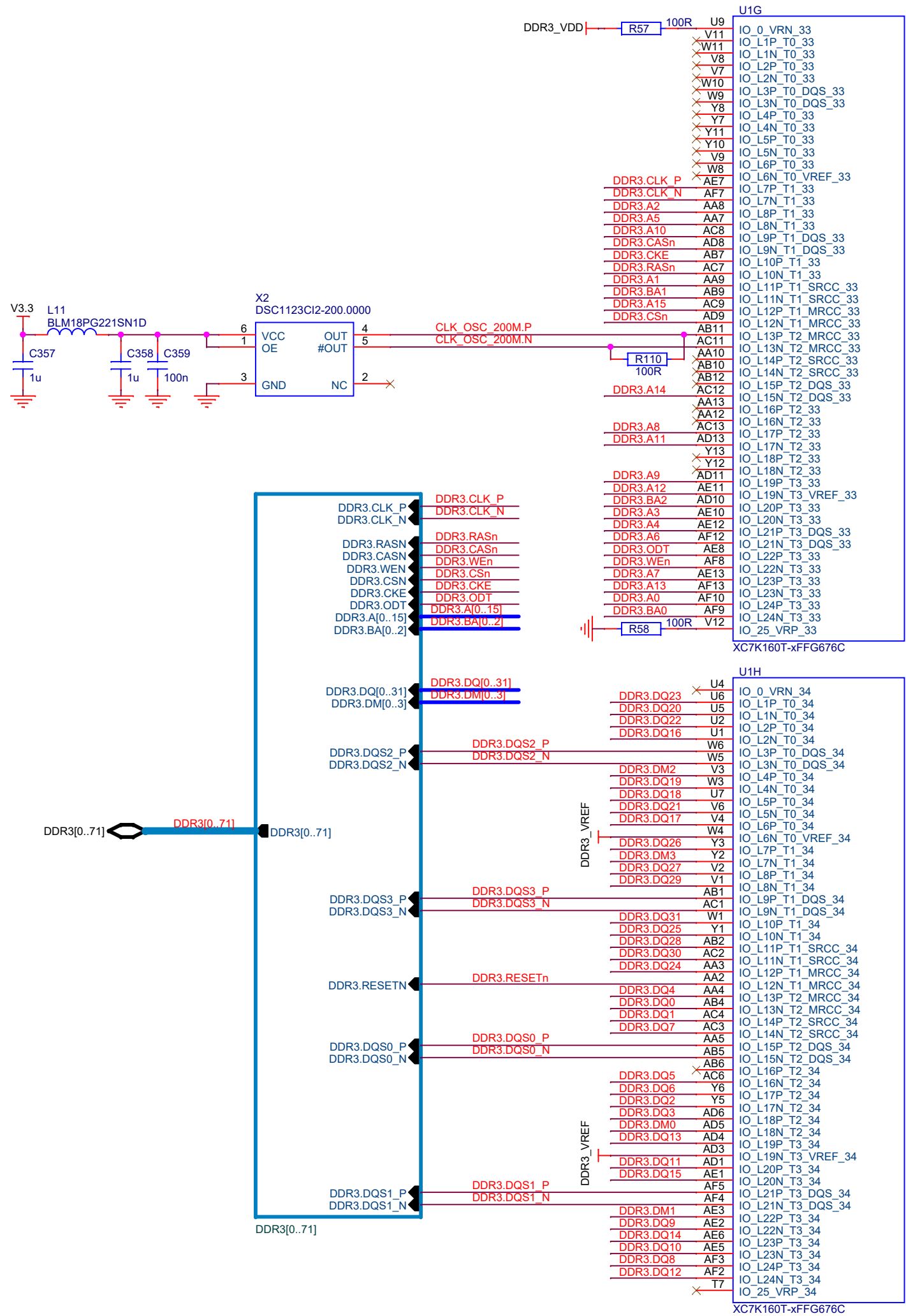
Input MUX	
CLK_SEL	Q[0:3]
L	CLK0
H (def.)	CLK1



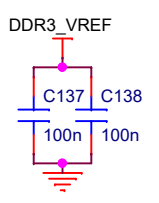
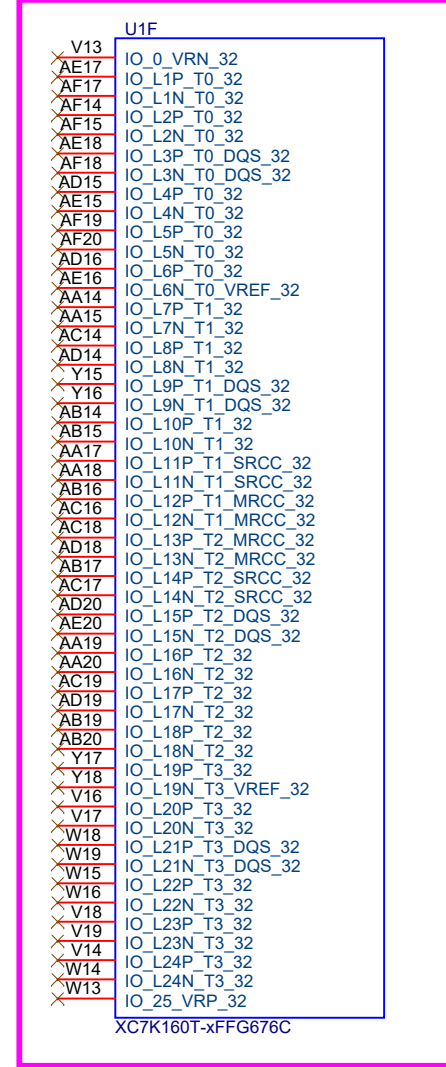


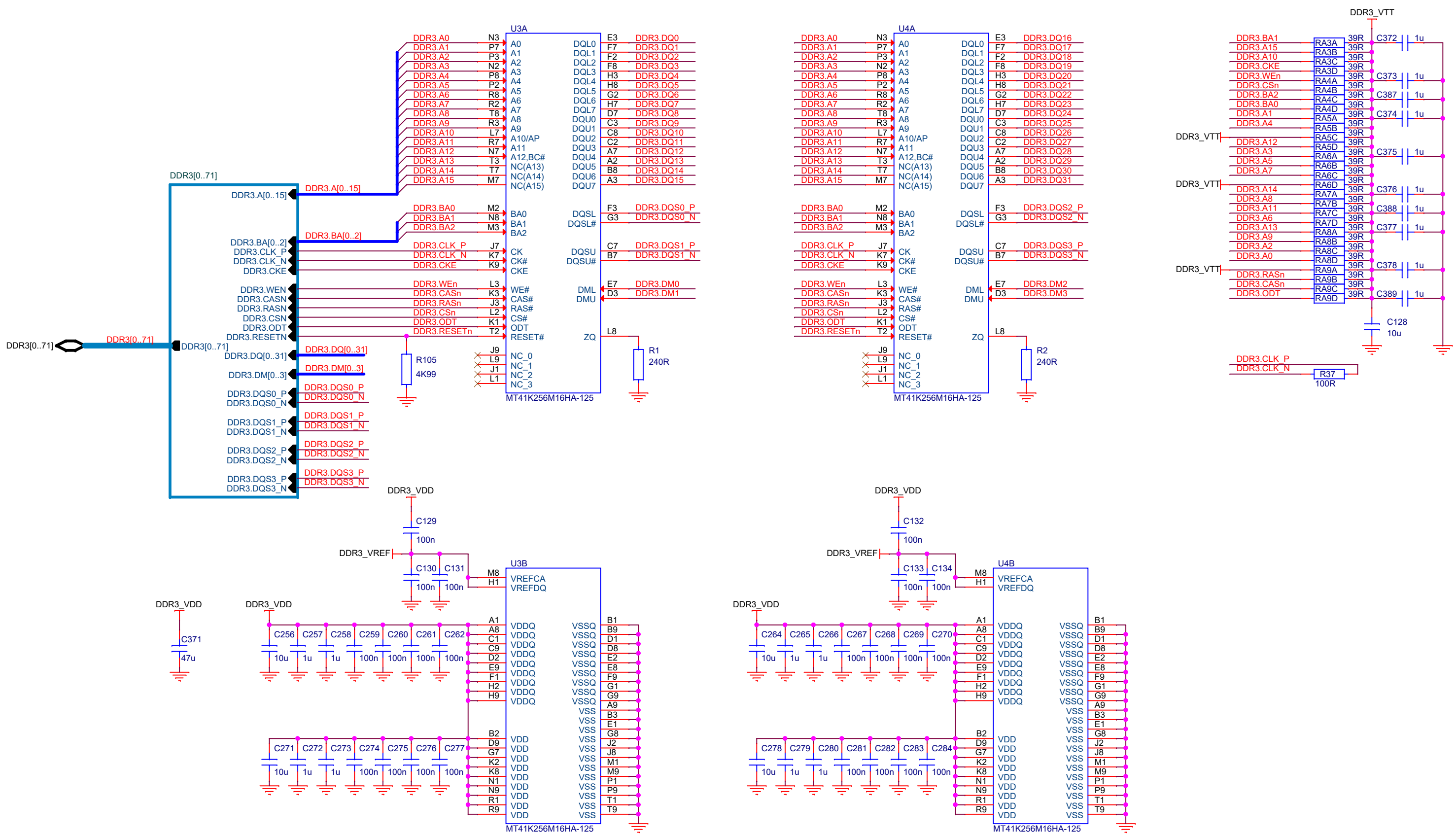
**XC7K70T:
IOB12 NOT CONNECTED**

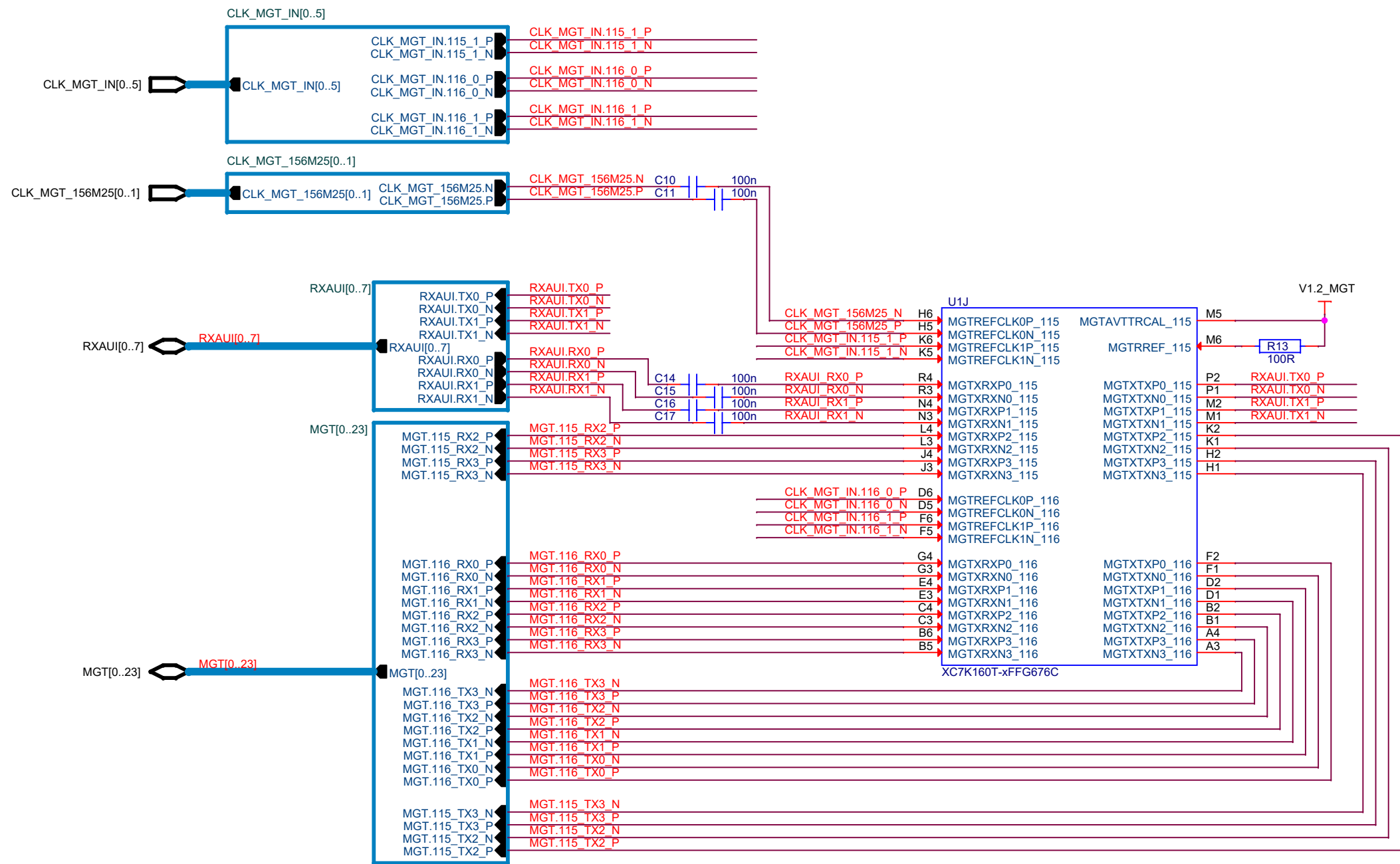


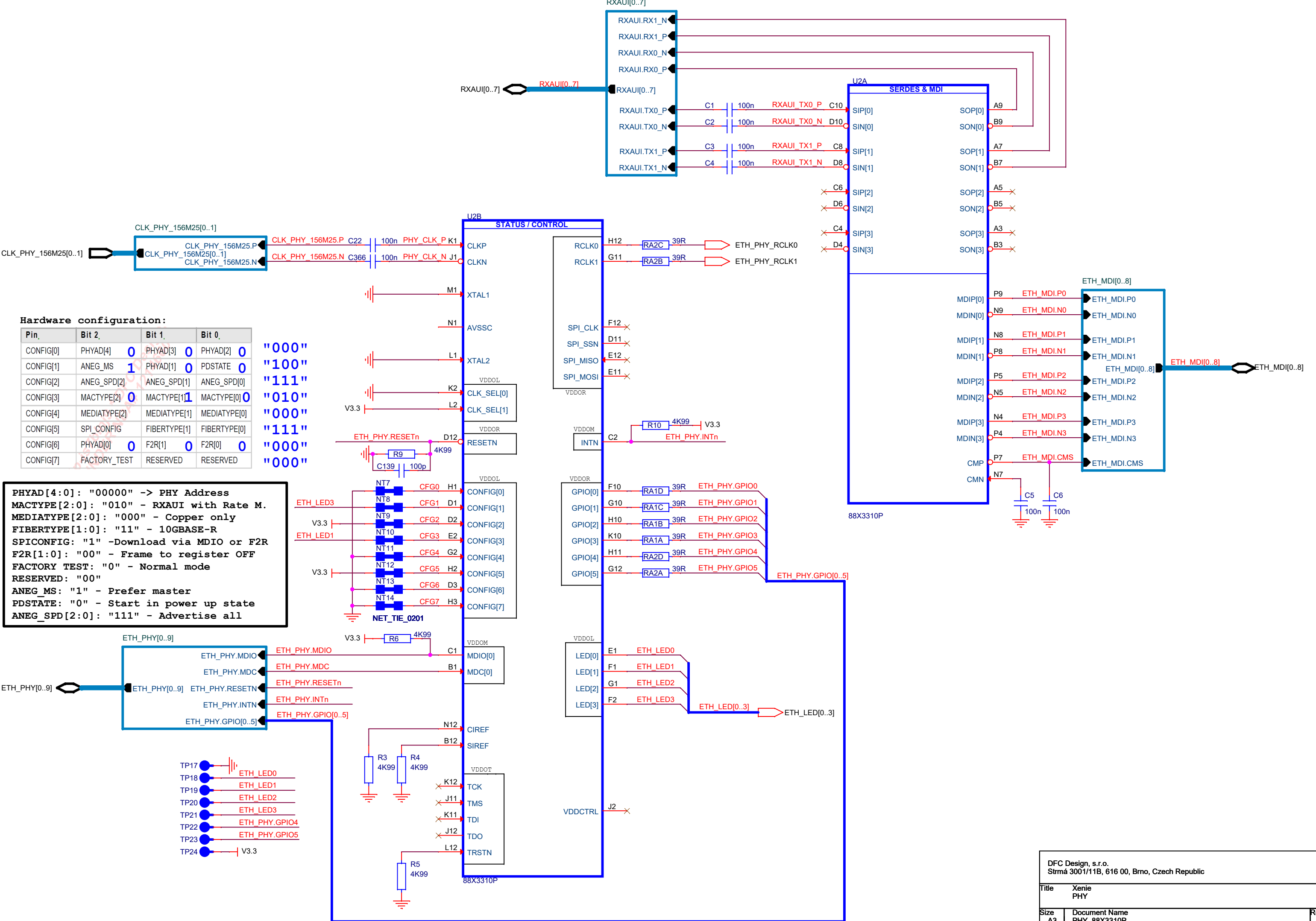


XC7K70T:
IOB32 NOT CONNECTED





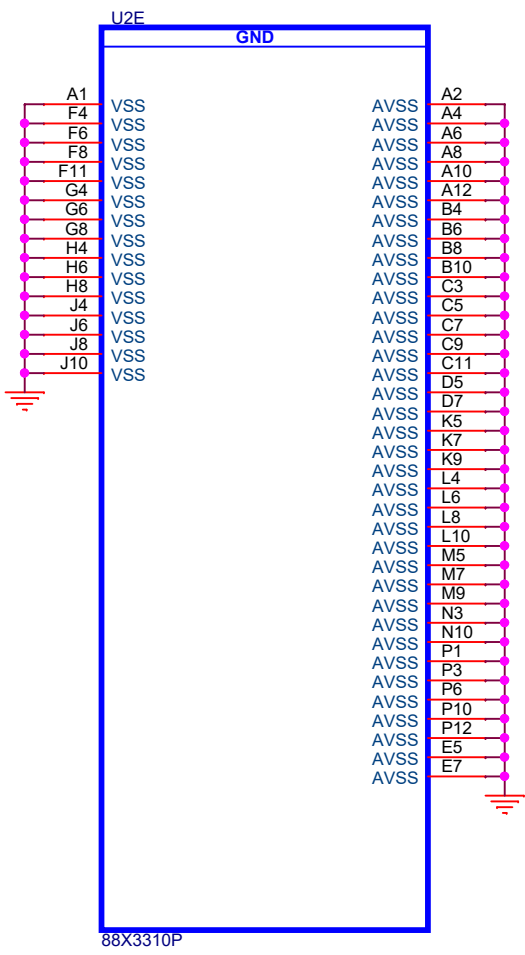
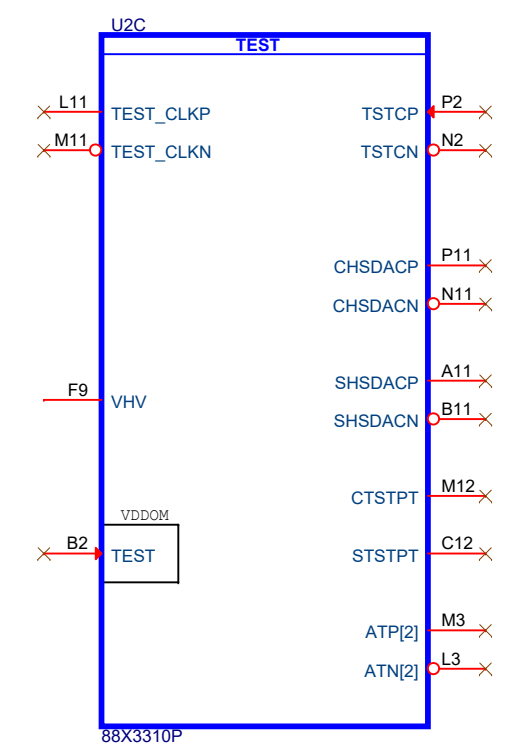
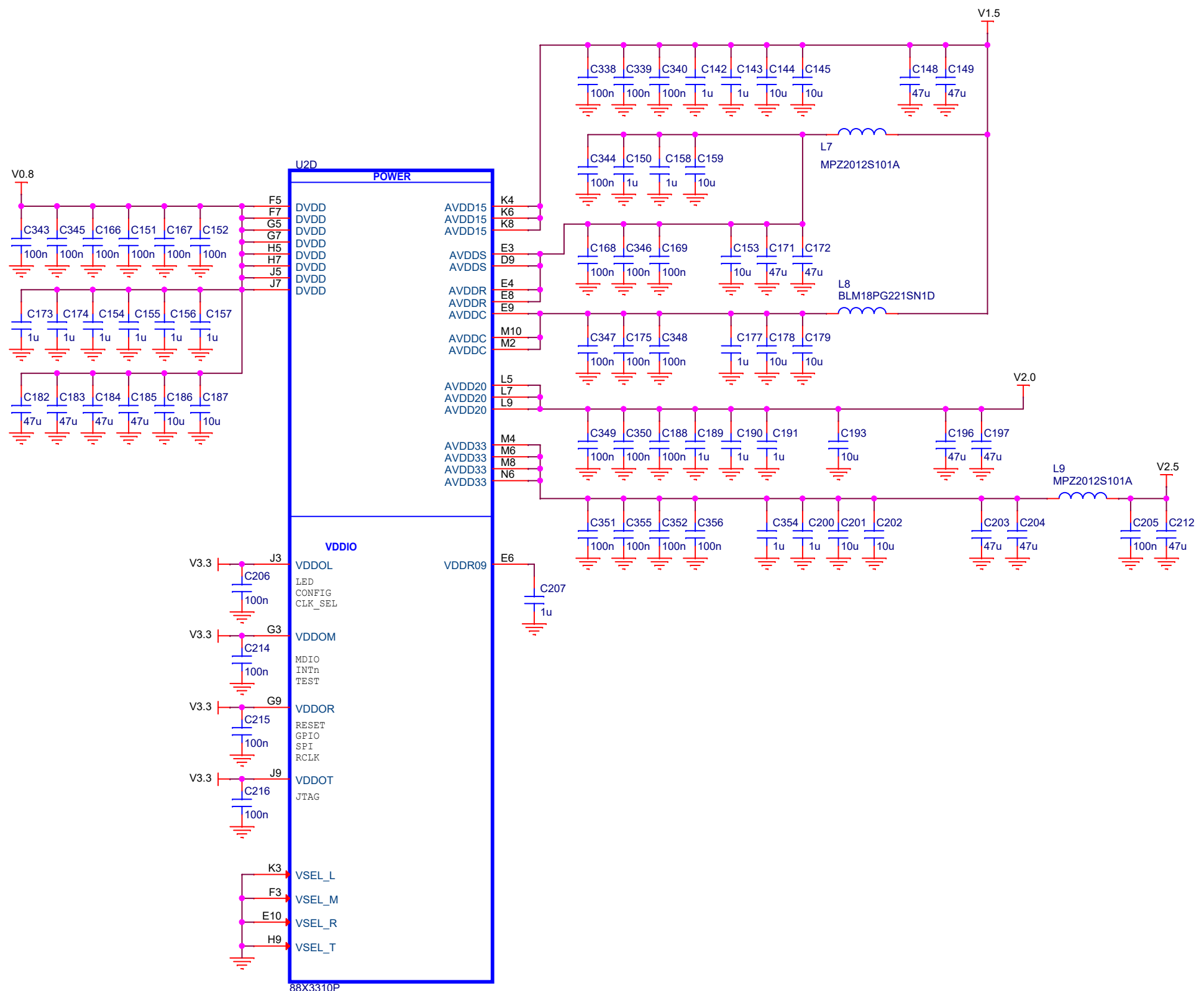




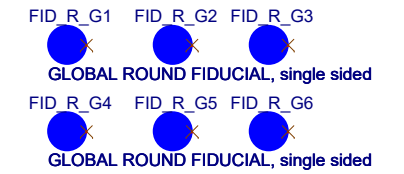
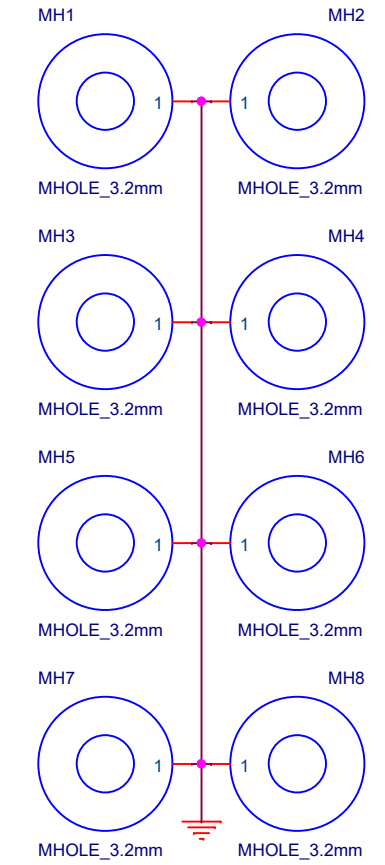
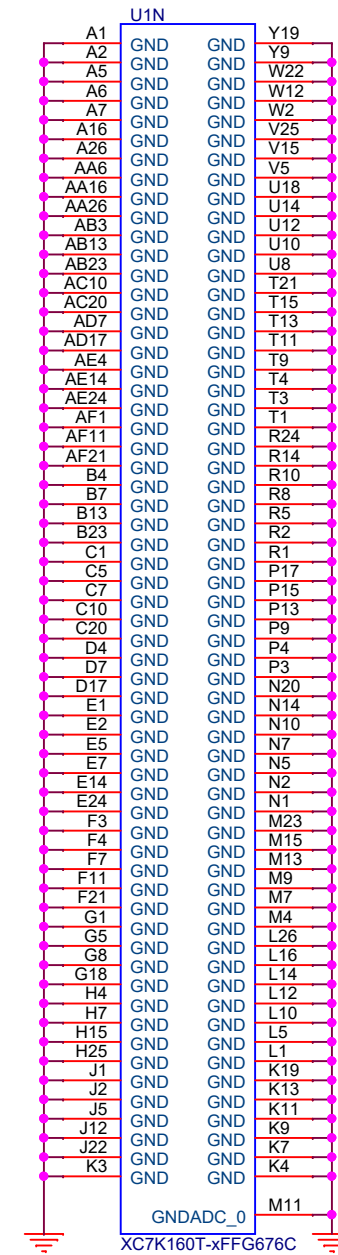
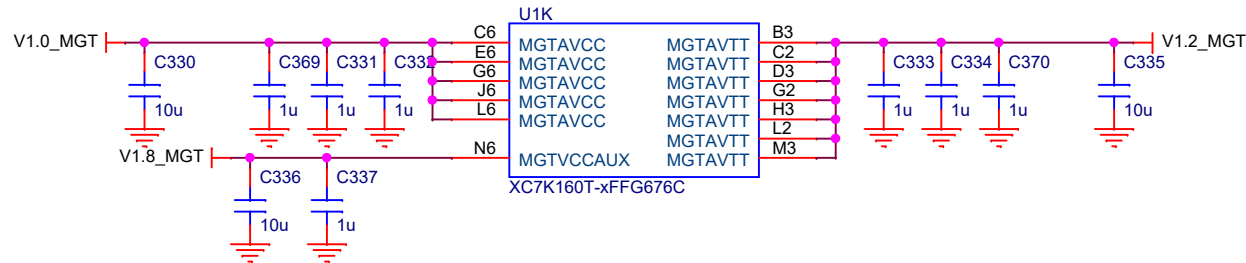
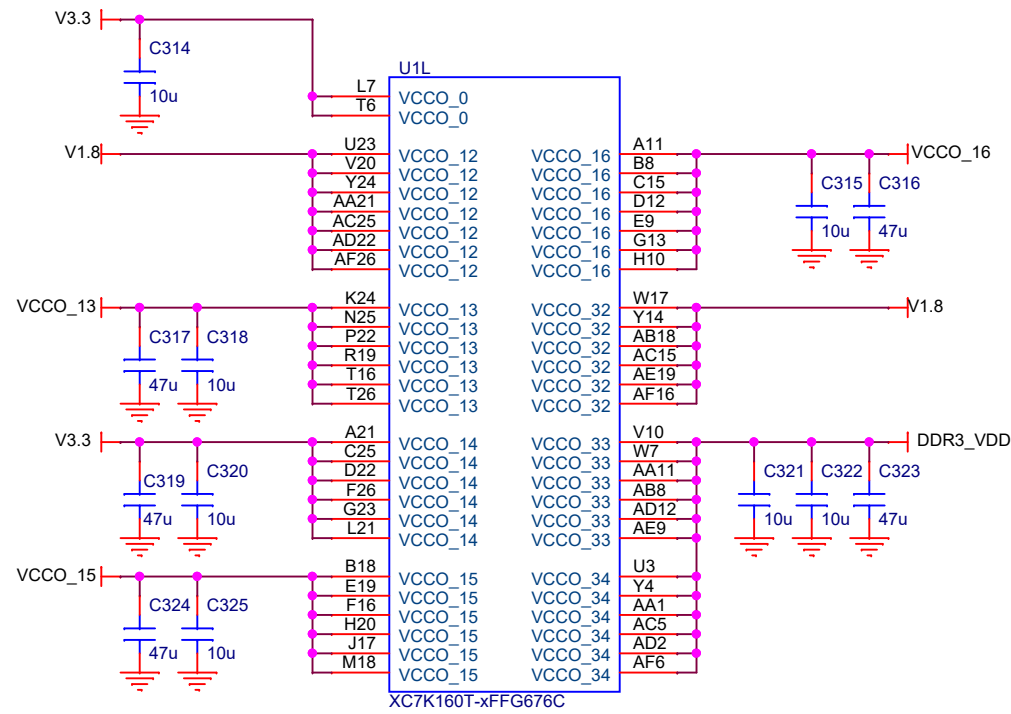
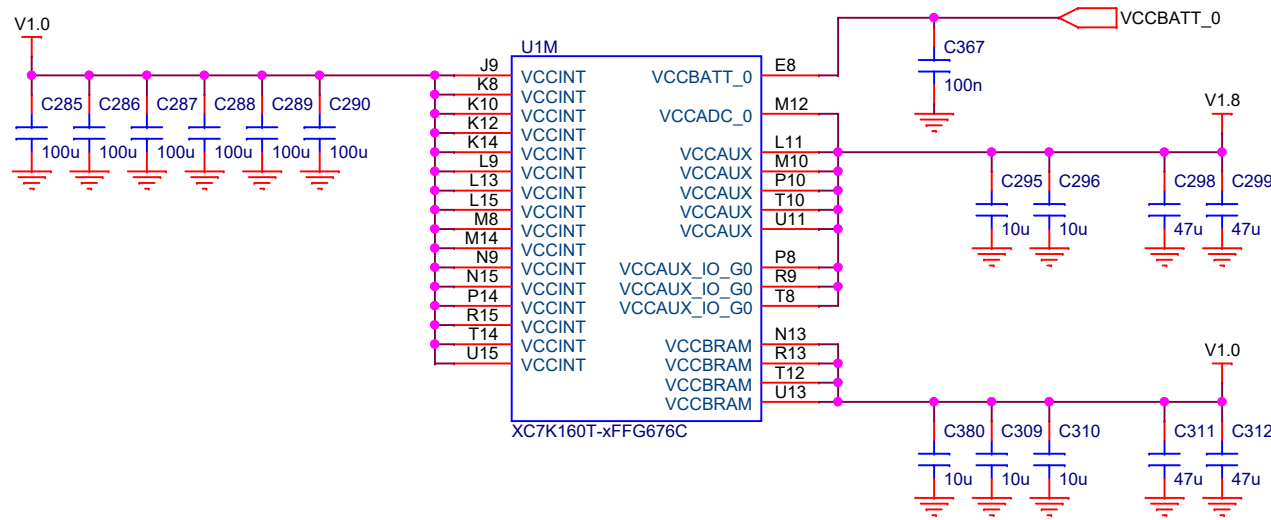
Hardware configuration:

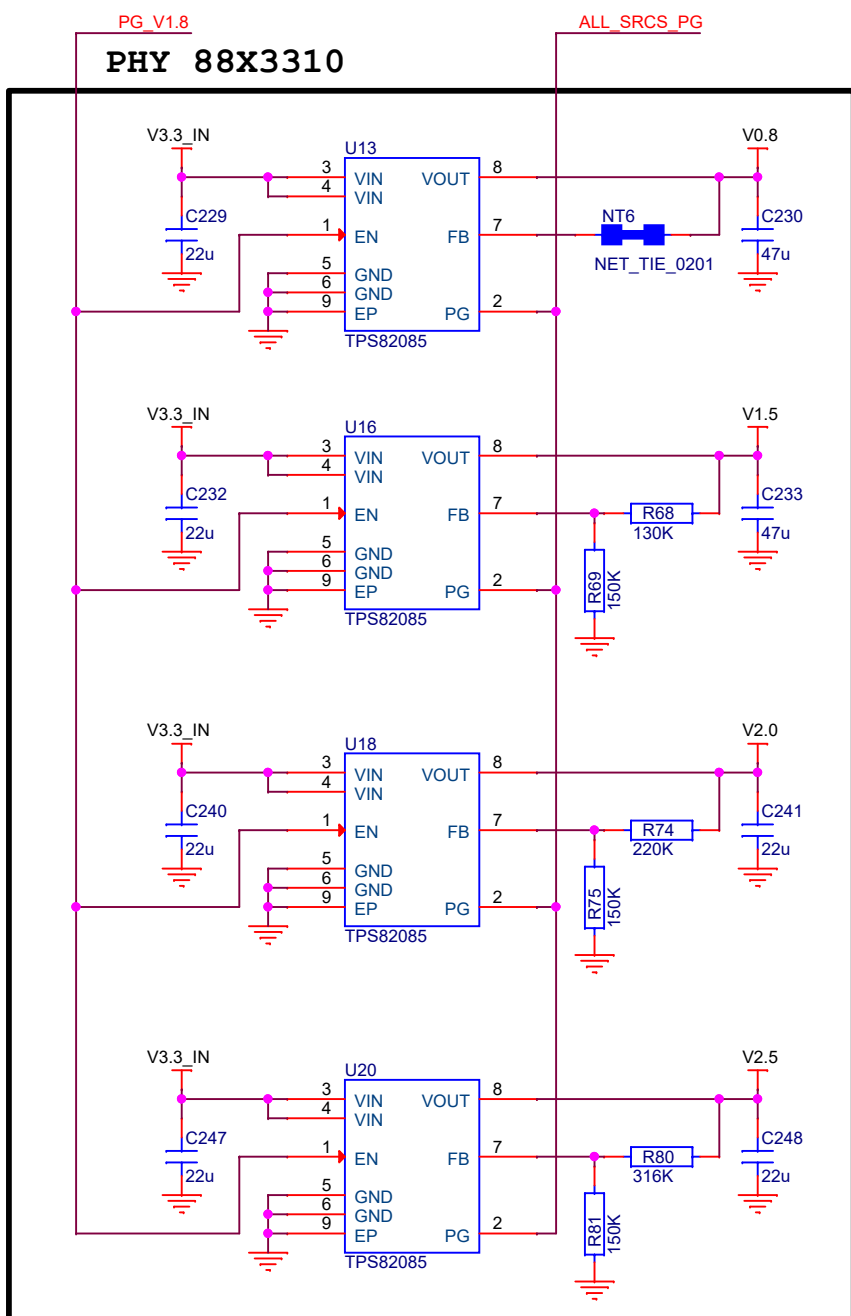
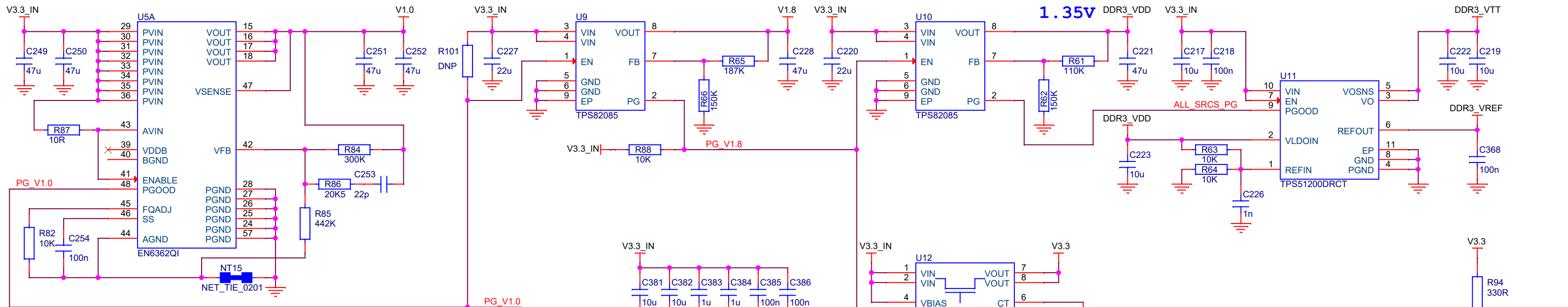
Pin	Bit 2	Bit 1	Bit 0				
CONFIG[0]	PHYAD[4]	0	PHYAD[3]	0	PHYAD[2]	0	"000"
CONFIG[1]	ANEG_MS	1	PHYAD[1]	0	PDSTATE	0	"100"
CONFIG[2]	ANEG_SPD[2]		ANEG_SPD[1]		ANEG_SPD[0]		"111"
CONFIG[3]	MACTYPE[2]	0	MACTYPE[1]	1	MACTYPE[0]	0	"010"
CONFIG[4]	MEDIATYPE[2]		MEDIATYPE[1]		MEDIATYPE[0]		"000"
CONFIG[5]	SPI_CONFIG		FIBERTYPE[1]		FIBERTYPE[0]		"111"
CONFIG[6]	PHYAD[0]	0	F2R[1]	0	F2R[0]	0	"000"
CONFIG[7]	FACTORY_TEST		RESERVED		RESERVED		"000"

PHYAD[4:0]: "00000" -> PHY Address
MACTYPE[2:0]: "010" - RXAUI with Rate M.
MEDIATYPE[2:0]: "000" - Copper only
FIBERTYPE[1:0]: "11" - 10GBASE-R
SPICONFIG: "1" -Download via MDIO or F2R
F2R[1:0]: "00" - Frame to register OFF
FACTORY TEST: "0" - Normal mode
RESERVED: "00"
ANEG_MS: "1" - Prefer master
PDSTATE: "0" - Start in power up state
ANEG_SPD[2:0]: "111" - Advertise all



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FPGA_MGT

